Materials Requirements and Fabrication of Active Matrix Arrays of Organic Thin-Film Transistors for Displays

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An overview of the materials requirements and the fabrication processes for the use of organic thin-film transistors in active-matrix backplanes for displays is presented. A summary of current knowledge of the electrical performance of both molecular and polymeric semiconductors is discussed with emphasis on the performance requirements needed for displays. Patterning and deposition processes for conductors, dielectrics, and organic semiconductors that have been used to fabricate organic thin-film transistors are reviewed. Examples of backplanes fabricated with these processes are given, and directions for the future research are outlined.

Introduction

There is great interest in the use of organic semiconductors in active-matrix thin-film transistor (AM-TFT) backplanes for displays. Displays belong to a class of electronic devices referred to as large-area electronics (LAE), or "macroelectronics".[1] Large-area electronics comprises electronic devices that must be relatively large, when compared to a standard integrated chip (IC), to execute their function. The use of printing technologies for patterning and the use of organic semiconductors for TFTs should reduce the cost of fabrication of AM-TFT backplanes. The availability of low-cost AM-TFT backplanes will enable the development of low-cost displays, electric paper, and active signage.[2]

Organic semiconductors have potential advantages to inorganic semiconductors for LAE devices. The field effect mobilities of carriers in organic materials are similar to those in amorphous inorganic semiconductors and are adequate for use in TFTs in backplanes for displays.[3] Organic thin films are relatively easy to deposit over large areas without complex equipment, such as plasma-based vacuum reactors, and they can be formed at low temperatures. Polymeric semiconductors have better mechanical compatibility with flexible substrates than inorganic films. These properties have stimulated interest in the use of organic semiconductors in AM-TFT backplanes.

The adoption of organic materials as the electrically active materials in AM-TFT backplanes presents two main challenges. First, the performance of TFTs made with organic semiconductors must be well understood. Understanding their electrical behavior is challenging because the chemical structures of organic semiconductors are diverse and also because organic films may be disordered or polycrystalline.[3] Second, fabrication processes must be developed that are compatible with these materials. Inorganic materials are generally impervious to the organic solvents used in semiconductor processing;[4] most known organic semiconductors are not. These challenges present many opportunities for both fundamental and applied materials research.

We outline, first, the electrical requirements of AM-TFT backplanes for displays that use capacitively switchable media, such as liquid crystals. These requirements are important to understand because they provide a target for improvement in the electrical performance of organic TFTs (OTFTs). Second, we review the physics and design issues that determine the electrical performance of OTFTs. Last, we review methods for fabrication of AM-OTFT backplanes.

I. Requirements for a TFT Backplane

A. Array Design. An active matrix backplane is an electronic circuit comprising an array of pixels whose purpose is to control a displayed image.[5] The individual pixels contain a single TFT and an additional storage capacitor, C_{ST} (Figure 1), and are addressed through orthogonal buslines that transmit gate and data voltages. The gate voltages control the on and the off states of the TFTs in the pixels; the data are transmitted line by line to write the image during an interval referred to as a frame time f_R. In addition, the most widely used capacitive display media require the electrical charge at the pixel to be retained while data are written to the other pixels.

Because the electrical signals to a backplane are time dependent, its electrical response is in part governed by its RC time constants.[5] The RC time constant for charging the pixel is given by eq 1, where R_{on} is the resistance of the TFT in the pixel (and assuming C_{ST} dominates the capacitance of the pixel).

$$T_{RC} = R_{on}C_{ST} \quad (1)$$

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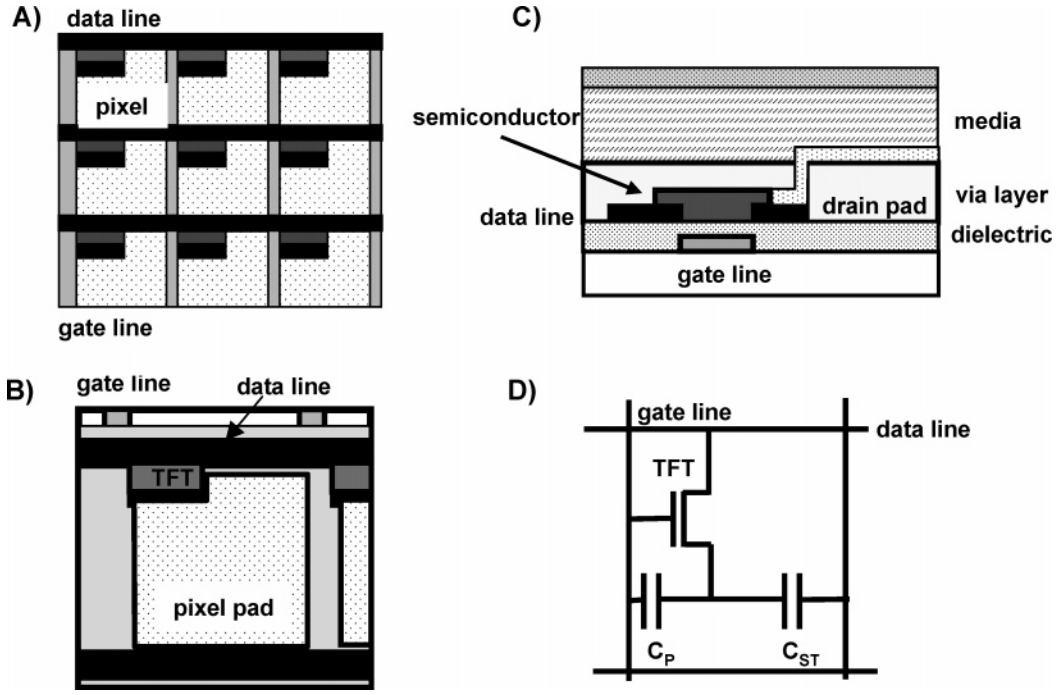


Figure 1. (A) Schematic of an AM-TFT backplane. (B) Top view of an individual pixel. (C) Side view of an individual pixel (not to scale for clarity). (D) Simplified electrical diagram of a pixel in a backplane.

Once programmed, the charge is retained at the pixel with a characteristic time constant T_{RET} given by eq 2, where R_{off} is the resistance of the pixel TFT in its off-state and R_{med} is the resistance of the imaging medium (e.g., liquid crystal cell).

$$T_{RET} = \frac{R_{med} \times R_{off}}{R_{med} + R_{off}} \times C_{ST} \tag{2}$$

The retention ratio r is defined as the fraction of retained charge at the pixel during the frame time (eq 3).

$$r = \exp\left(-\frac{1}{T_{RET} \times f_R}\right) \tag{3}$$

Finally, the RC time constant of the address lines is given by eq 4, where R_{PL} and C_{PL} are the resistance and capacitance of the metal line for one pixel, and N is the number of lines in the array.

$$T_{RC-ADD} \approx N^2 R_{PL} C_{PL} \tag{4}$$

Because of capacitive coupling between the gate line and the pixel, the data voltage at the pixel is reduced by an amount equal to the feed-through voltage V_{FT} (eq 5), where C_P is the parasitic capacitance coupling the gate line to the pixel and V_G is the gate voltage relative to the pixel voltage.

$$V_{FT} = V_G C_P / C_{ST} \tag{5}$$

During operation, each gate line must be turned on to charge the pixel for a minimum time that is a multiple of T_{RC} (e.g., $5T_{RC}$). A retention rate $r = 0.99$ is typically required for the display to work properly. If we assume $N = 600$ lines and a 60 Hz refresh rate, the current required to charge a pixel can be calculated. Using a pixel programming voltage $V_D = 10$ V, $C_{ST} = 1$ pF, and $R_{med} = 10^{13}$ Ω, we obtain $I_{on} > 1.8$ μA and $I_{off} < 5$ pA. Larger displays impose more stringent requirements on the materials. For instance, increasing N while keeping f_R constant (e.g., video rate) requires a shorter T_{RC} and hence a smaller R_{on} (higher I_{on}). Moreover, the N^2 dependence in T_{RC-ADD} quickly increases the time constant of the addressing lines. Typical values for metallic electrodes are $C_{PL} \approx 1-5$ pF and $R_{PL} \approx 1-10$ Ω, or $R_{PL} \approx 10-100$ kΩ for conducting polymers (assuming a thickness of ~100 nm). With metals, the time constant is small enough to drive displays with $N = 1000$, but it is not with conducting polymers. These requirements, of course, depend on the functionality of the display. For instance, if a display uses bistable media, for example, electrophoretic particles, it may be refreshed less frequently (~1 Hz) and the time constants could be larger.

B. Transistor Design. The resistance of the active part of the TFT, the channel, is modulated by the voltage of the gate electrode (see Figure 2). Most OTFTs operate as p-type accumulation mode devices. The transistor is turned on by increasing the hole concentration in the channel (N_{CH}), which is controlled by the voltage of the gate electrode (V_G), the threshold voltage (V_T), and the capacitance/area of the gate dielectric (C_0).

$$N_{CH} = C_0 |V_G - V_T| \tag{6}$$

A p-type accumulation device is turned on when $(V_G - V_T) < 0$. The threshold voltage is mostly controlled by localized states and trapped charge at the dielectric/semiconductor interface. The drive current flowing between the source and drain, I_D, of the transistor in the linear regime ($|V_{SD}| < |V_G - V_T|$) predicted in the gradual channel approximation is given by eq 7, where

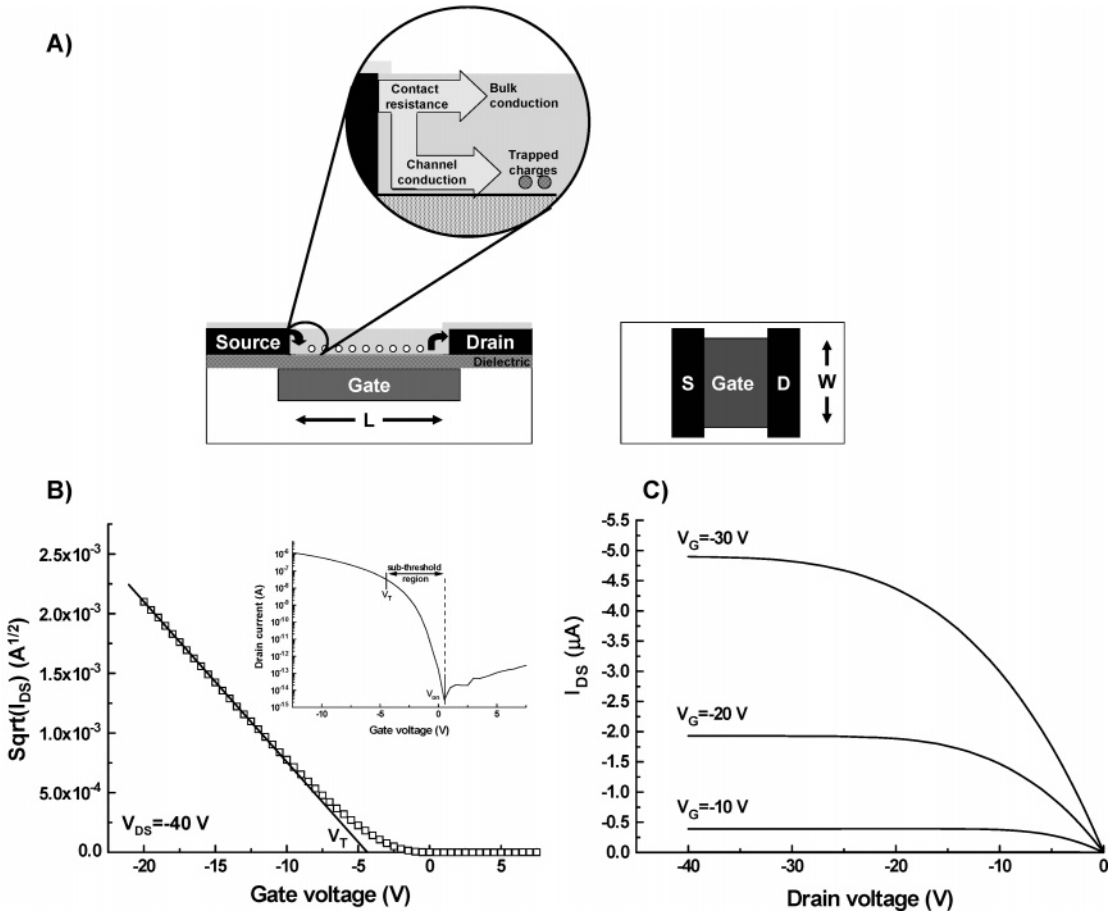


Figure 2. (A) Coplanar thin-film transistor structure. In a p-type accumulation device, holes are injected at the positively biased contact (source). Channel conduction is affected by trapping at the dielectric interface. Bulk conduction determines I_{off}. (B) Typical transfer and (C) output characteristics of a well-behaved (e.g., little bias stress and low contact resistance) polymeric TFT.

μ is the carrier drift mobility and W and L are the device dimensions (Figure 2).[6]

$$I_{SD} = \frac{W}{L}\mu C_0\left(V_G - V_T - \frac{V_{SD}}{2}\right)V_{SD} \quad (7)$$

When $|V_{SD}| > |V_G - V_T|$, the transistor operates in saturation regime. The drive current in saturation is independent of V_{SD}, and eq 7 simplifies into eq 8.

$$I_{SD} = \frac{W}{2L}\mu C_0(V_G - V_T)^2 \quad (8)$$

From eq 7, we can derive the on-resistance of the transistor in the linear regime, including the contact resistances R_C at the source and drain (eq 9).

$$R_{on} = R_C + \left[\frac{W}{L}\mu C_0\left(V_G - V_T - \frac{V_{SD}}{2}\right)\right]^{-1} \quad (9)$$

The off-resistance of the transistor is limited by leakage currents and by the residual carrier concentration when the device is turned off (i.e., $(V_G - V_T) > 0$).

C. Pixel Design. A good pixel design minimizes T_{RC} to allow for fast addressing and also minimizes V_{FT}. Increasing C_{ST} reduces V_{FT} and increases T_{RET} at the cost of increasing T_{RC}. The design goals are met by simultaneously minimizing the on-resistance of the TFT, R_{on}, and the parasitic capacitance, C_P. Moreover, a large R_{off} is needed to maximize T_{RET}.

II. Design and Materials Requirements for OTFTs

A. On-Resistance. As shown in eq 9, R_{on} has two components: the channel resistance, which is modulated over several orders of magnitude by the gate voltage, and the contact resistance. The channel resistance can be minimized in principle by pursuing aggressive transistor designs (i.e., large W/L). Using a small L, however, can be problematic because of nonideal electrical behavior arising in short-channel devices (<5 μm).[6] On the other hand, W cannot be increased arbitrarily without a loss of optical fill factor in backlit displays. Thus, for a given transistor design (i.e., W/L), one must determine minimum requirements for the carrier drift mobility μ and the threshold voltage V_T of the organic semiconductor. These minimum requirements will, of course, depend on the design rules of the display. For instance, mobilities as low as $\sim 10^{-3}$ cm^2/(V s) have been successfully used in AM-OTFT backplanes for reflective media because a large W/L was used.[7,8]

Carrier Mobility in Organic Semiconductors. The mobility of carriers in organic semiconductors[3] is several orders of magnitude lower than that in inorganic crystalline materials and is comparable to hydrogenated amorphous silicon, a-Si:H.[9] Organic semiconductors can be divided in molecular crystals and polymers where the former are usually vacuum-sublimed to form thin films while the latter are deposited from a solution. To date,

the highest mobility reported, 8 $cm^2/(V\ s)$, was observed in a single-crystal rubrene transistor.[10] The highest values for transistors made from thin films are ~5 $cm^2/(V\ s)$ for polycrystalline pentacene[11] and ~0.1 $cm^2/(V\ s)$ for poly(3-hexylthiophene), P3HT,[12] and poly[5,5′-bis-(3-dodecyl-2-thienyl)-2,2′-bithiophene], PQT-12.[13]

The lower mobility of organic crystals as compared to inorganic crystals is attributed to the weak intermolecular forces that limit charge transport. This weak interaction causes hopping to be a dominant mechanism of transport. In films of both crystalline and polymeric organic semiconductors, the presence of nonmobile electronic states, or traps, also limits the mobility. It is important to remember that the electrostatics of a field-effect device cause the current to flow very close to the dielectric/semiconductor interface.[6] In TFTs, therefore, the mobility is not exclusively a property of the isolated semiconductor but should rather be viewed as a property of the semiconductor/dielectric interface.

Molecular Order and Transport Properties. Electrical transport in organic semiconductors is inherently anisotropic at the molecular scale: charges are delocalized within the molecules (or within the conjugation length along the backbone of a polymer), but the rate-limiting step of transport is the intermolecular (or interchain) hopping of the charges. In a rubrene single crystal, this anisotropy has been observed directly by measurements of the field-effect mobility along different crystalline axes.[14] Intermolecular hopping is most effective when the structural order of the material maximizes the overlap of the π orbitals. Therefore, structures that produce strong $\pi-\pi$ orbital overlap should generally lead to higher carrier mobilities than those that do not.

Polycrystalline films of molecular semiconductors, such as oligothiophenes and polyacenes, tend to have higher carrier mobilities than amorphous films.[3] The size of the crystalline regions affects the observed mobility of polycrystalline films. Scanning probe studies of oligothiophenes and polyacenes have shown that grain boundaries in polycrystalline films constitute barriers to charge transport[15] and can reduce the apparent mobility of an OTFT.

Studies of semiconducting polymers have shown that the highest field-effect mobilities are also related to ordered phases. Two ordering mechanisms are observed. In the first, polymer molecules can be oriented by heating to a liquid-crystalline phase. The use of this ordering was demonstrated to improve transport and cause an anisotropy in the mobility of a film of poly(fluorene-*co*-bithiophene), F8T2.[16] Liquid-crystalline order only involves the polymer backbone and does not necessarily maximize $\pi-\pi$ overlap. It is speculated that the anisotropy may be due to a longer average diffusion distance per interchain hop when the polymer chains are oriented parallel to the current flow. In the second ordering mechanism, a polymer may form a polycrystalline film where the crystalline grains are separated by amorphous regions (e.g., regioregular poly(thiophenes)).[12,13] The crystallinity of the film, the orientation, and the size of the crystalline grains are functions of the film casting process and of the degree of regioregularity of the polymer. For poly(thiophenes), the polymer chains are organized in a lamellar structure within the grains, and the $\pi-\pi$ overlap direction is perpendicular to the individual lamellae. The highest mobility for a P3HT-based TFT was obtained when the lamellae were perpendicular to the dielectric surface, allowing $\pi-\pi$ overlap in the plane of the current flow.[12] The effective mobility of the film, however, is also affected by the disordered regions between the crystalline grains, which have a role similar to that of grain boundaries in molecular crystals and can act as trapping sites.

Dielectric/Semiconductor Interface Energy and Transport Properties. An absolute correlation between structural order and the mobility measured from TFTs is not always observed because interfacial interactions at the semiconductor/dielectric boundary affect device performance. The role of these interactions has been studied by modifying the interface in a controlled fashion. The most commonly used method is to chemically functionalize the dielectric surface with a self-assembled monolayer (SAM), for example, alkyltrichlorosilanes on SiO_2 or alkylphosphonic acids on Al_2O_3, prior to the deposition of the semiconductor.

A number of studies have demonstrated that modification of oxide dielectrics with SAMs leads to pentacene TFTs with mobilities of 1 $cm^2/(V\ s)$ and larger.[17−19] If appropriately chosen, these SAMs form ordered films at the surface of the dielectric and dramatically lower its surface energy. Interestingly, ordering of the interfacial coating may not be essential because high-performance pentacene films, $\mu \approx 5$ $cm^2/(V\ s)$, have been made on dielectrics coated with an ultrathin poly(styrene) layer.[11] Despite their high mobility, some pentacene films deposited on SAMs on SiO_2 have smaller grain sizes than those deposited on the bare dielectric.[18] The increased mobility can be due to factors unrelated to grain size. For instance, the effect of the presence of multiple crystalline polymorphs and the effect of grain boundary orientation on semiconductor properties remain unknown.

Modifying the dielectric surface energy affects the mobility of polymer semiconductors as well. Hexamethyldisilazane (HMDS) treatment of the dielectric surface increases the mobility of P3HT by a factor of 2.[12] Using SAMs such as OTS leads to an even more pronounced effect in F8T2 where the mobility of the semiconductor is enhanced by a factor of approximately 20.[20] Experiments conducted on chemically functionalized dielectric surfaces indicate that the semiconductor mobility does not depend simply on surface energy or on the presence of apolar groups at the dielectric interface. The mechanism leading to the improvement in mobility is not completely understood, but it is likely to be linked to molecular interactions between the semiconductor and treated dielectric surface.

It is difficult to uncover the mechanism by which a chemically functionalized dielectric surface causes changes in the mobility of OTFTs. Because charge flows in approximately the first molecular layer of the semiconductor at the dielectric interface, bulk characterization techniques that are routinely used (e.g., X-ray diffraction and polarized light absorption spectroscopy) do not always provide relevant information.

Threshold Voltage. The threshold voltage of a TFT determines where the device switches from its off-state to its on-state; control of V_T is necessary to build an AM-

TFT backplane. Ideal TFTs turn-on sharply when $V_G = V_T$, and eqs 7 and 8 only strictly apply when devices are in their on-state. Current actually flows through a TFT at voltages below threshold; the voltage where these first mobile charges are induced is called the onset voltage V_{on}. In the subthreshold region, that is, the regime of operation between V_{on} and V_T, the TFT current is low and varies approximately exponentially with V_G. It is desirable to have as small a subthreshold region as possible because the induced charges in this region primarily fill nonmobile trap states instead of mobile states.[9]

A TFT with a semiconductor that has few trap states and a good semiconductor/dielectric interface turns on near 0 V. On the other hand, residual doping in the semiconductor, fixed charge, and dipoles at the dielectric interface can cause V_{on} to vary over a range of several tens of volts. Doping of the semiconductor can be due to the presence of residual impurities (e.g., inorganic catalysts from synthesis) or interaction with the environment. Fixed charges at the semiconductor/dielectric interface can be due to mobile ionic impurities in the semiconductor or the dielectric, impurities on the dielectric surface prior to the deposition of the semiconductor, or uncompensated bonds and charged trap states on the dielectric surface. Shifts of V_{on} have also been observed in dielectric surfaces functionalized with polar SAMs.[20] OTFTs with high carrier mobility, but extremely high V_{on}, ~40 V or more, have been previously reported.[21] While in principle, the operating V_G range of the driving electronics of the AM backplane can be programmed to compensate for large V_{on} offsets, it is generally preferable to operate at small voltages ($<|30|$ V). Use of purified semiconductor and dielectric materials, control of their deposition processes, and cleanliness during TFT fabrication usually results in a low V_{on}, in the absence of environmental doping. In the discussion that follows, we will focus on V_T, and we will assume that $V_{on} \approx 0$ V has been achieved.

To take best advantage of the operating V_G range, it is desirable to minimize $|V_T|$ because the difference between V_G and V_T determines the current in a TFT (eqs 7 and 8). To obtain a small V_T, it is necessary to minimize the number of shallow donor-like trap states that are energetically close to the mobile states because these states are filled when V_G sweeps the subthreshold region.[9] In polycrystalline semiconductors, these states are often associated with grain boundaries and amorphous regions between the grains. Threshold voltages of the order of a few volts are commonly reported thanks to good control over the structure and morphology of the semiconductor material. For polymeric semiconductors, Baessler has suggested that these states are inherently associated with the disordered nature of polymeric films.[22] Indirect measurements of the concentration and energy distribution of these states have been obtained by measuring TFT characteristics as a function of temperature.[23−25] Typical trap densities are $\sim 10^{20}$ cm^{-3} with an energetic distribution width that varies between ~10 and 40 meV. It is expected that a decrease in ordering should lead to larger concentrations and wider distributions of these donor-like states.

Contact Resistance. Operating a TFT involves injecting charge from the electrodes into the organic semiconductor. To first order, the contacts can be described as a Schottky barrier between the metal and the semiconductor because, in general, the work functions (ϕ) of the two materials are mismatched. In p-type accumulation devices, the source electrode is a reverse-biased Schottky diode, while the drain electrode is a forward-biased diode.[6] More sophisticated models comprising antiparallel diodes in series with a resistance have also been proposed.[26]

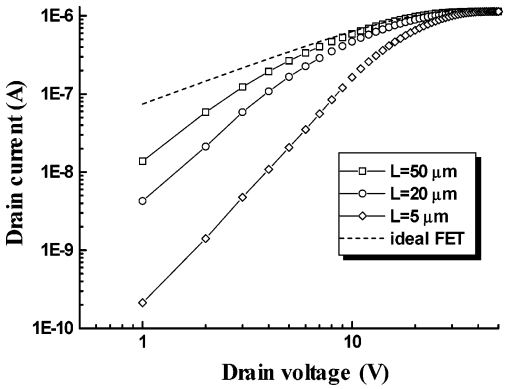


Figure 3. Drain current as a function of drain voltage for a poly(thiophene) TFT ($V_G = -40$ V) as a function of channel length L in a coplanar device. Contact effects are visible at low drain voltage. The effect of the contact resistance is relatively more important as the channel length becomes smaller.

Several methods can be used to extract the contact resistances of a TFT and generally rely on measurements of devices with different channel lengths (Figure 3). In the transmission line model (TLM), the contact resistance is determined by extrapolation of eq 9 to $L = 0$.[6] An implicit assumption of this method is that the contact resistance is approximately ohmic at low I_{DS}. Other methods relying on measuring drain conductance and transconductance have been used as well.[27] The most general method consists of fitting an $I(V_C)$ function to the output characteristics of the device, where V_C is the voltage drop at the contact due to the contact resistance.[28] The use of this method in coplanar polymeric TFTs indicated that the electrical characteristics of the contacts are indeed diode-like and quasi-ohmic behavior is observed when the overall resistance is small or at small I_{DS}.[28,29]

Injection of carriers into organic semiconductors is not as well understood as that into inorganic semiconductors. This situation is partially due to unknown material properties at the microscopic scale near the contact and to the physics of charge injection into a material where transport occurs by hopping. Although the injection efficiency in an organic semiconductor (defined as the ratio between the injected current and the space-charge-limited current) is independent of carrier mobility,[30] the absolute contact resistance decreases with increasing mobility. An empirical relationship between the contact resistance and the carrier mobility in polymer semiconductors has been observed.[31] In addition, the contact resistance is generally lower at higher gate voltage due to reduced screening of the gate voltage near the source electrode leading to a participation of the gate field in the injection process.

Contact resistance can depend on the geometry of the contacts.[26,29] In the staggered configuration, the contact area is larger and the electric field lines favor charge

injection, leading to a lowered contact resistance as compared to the coplanar configuration.[28] The coplanar geometry is, however, more desirable for its ease of fabrication and reduced risk of damage to the semiconductor from deposition of the electrodes.[26]

The best candidate electrode materials for hole injection in p-type organic semiconductors have a high work function. It is preferable that the electrode material does not form an insulating oxide layer at ambient conditions that can cause an additional injection barrier. The most commonly used electrodes are Au ($\phi \approx 5.2$ eV) and indium−tin−oxide (ITO) ($\phi \approx 4.1-5.5$ eV).[32] A blend of poly(3,4-ethylenedioxythiophene) and poly(styrene sulfonate), PEDOT/PSS, has also been used as a hole injection contact material because its work function is ~5 eV.[33] Its use in applications is, however, questionable because it tends to separate into its components and diffuse in the semiconductor under high voltages.[34] These values of ϕ are only approximate because they can be lowered by adsorption of organic molecules onto their surfaces, which will increase the injection barrier.[35]

Organic semiconductors are often designed to have a large ionization potential to reduce the driving force of oxidative doping, and, as a result, large injection barriers often exist between the contact and the semiconductor (e.g., Au/pentacene, 0.85 eV; Au/F8T2, 0.3 eV).[29,35] Using scanning probe techniques, Bürgi et al.[29] have shown that when a large difference in ϕ (~0.3 eV) exists between the electrode and the semiconductor, hole injection is more difficult than hole extraction. When the difference is low (<0.1 eV), the potential drop is the same at the source and the drain. This observation is explained by the existence of a "bulk" resistance region near the contacts independent of the polarity of the electrodes.

Contact resistances affect TFT performance noticeably when they become comparable to the channel resistance. Measured contact resistance values vary with contact material and preparation method, measurement conditions, material morphology, and mobility. Some approximate values are 10 kΩ cm for Au/pentacene,[36] 100 kΩ cm for Au/oligothiophene,[27] and 10 kΩ cm for P3HT with $\mu = 0.05$ cm^2/(V s).[31] The critical device length where the channel resistance is equal to the contact resistance can be calculated according to eq 9 for typical operating conditions ($C_0 \times |V_G - V_T| \approx 4 \times 10^{12}$ cm^{-2}) and is approximately 3 μm for a polymer device with $\mu = 0.05$ cm^2/(V s).

B. Off-Resistance. The off-resistance, R_{off}, cannot be simply expressed in a closed equation form similar to eq 9 as it depends on the properties of the semiconductor and the design of the backplane. For instance, the main purpose of semiconductor patterning is to minimize leakage currents due to ungated material or, equivalently, an increase in R_{off}. Moreover, TFTs must be designed to minimize possible low resistance paths (e.g., ungated semiconductor edges).

To turn the TFT off, the semiconductor material must be completely depleted of mobile charge. Thus, to obtain a high R_{off}, the depletion layer in the semiconductor must be at least equal to the thickness of the semiconductor when the gate voltage is set to the off-value V_{off} (a positive value of $(V_G - V_T)$ for p-type TFTs). Acceptor-like states cause residual conduction at $V_G > 0$; hence for a given $V_{off} > 0$ there is a maximum acceptor density that allows depletion of the semiconductor throughout its whole thickness.[37] Acceptor-like states in organic semiconductors are typically due to residual impurities or to environmental doping by O_2 or H_2O. Meijer et al. have measured the increase in acceptor concentration in poly(2,5-thienylene vinylene) (PTV) and P3HT upon exposure to air.[37] P3HT, in particular, is known to form a charge-transfer complex with O_2 that leads to doping.[38]

R_{off} is also sensitive to electrically active residual impurities in the material such as metal ions leftover from the material synthesis. Ionic current is independent of the gate voltage and contributes thus to I_{off}. In general, control over material purity (i.e., doping) and accidental contamination is sufficient to obtain a high R_{off} in most organic semiconductors.

C. Stability of Electrical Characteristics. The characteristics of the TFTs used in backplanes must be reliably predictable. The I−V characteristics of an ideal TFT remain unchanged regardless of the bias voltages and bias times. Bias stress is a nonideal behavior in TFTs where the threshold voltage of the TFT varies as a function of gate bias. Bias stress is detrimental because it limits the useful range of the transistor. $I-V$ data from TFTs obtained at low carrier concentrations neglect bias stress, and they cannot be reliably extrapolated to operation at higher carrier concentration. Learning how to control and predict bias stress was a fundamental step in the development of a-Si:H AM-TFT backplanes.[9]

Bias stress has been observed in both molecular and polymeric semiconductors.[18,39−42] In pentacene-based TFTs, a threshold voltage shift of the same sign as the gate bias is observed after either positive or negative gate bias. The transfer characteristics recover after several hours, and illumination does not accelerate the recovery process.[18] It has been proposed that bias stress in pentacene is due to hole trapping in an electronic state generated by hydrogenated or oxygenated molecules of pentacene.[43]

Threshold voltage shifts due to charge trapping and Na^+ diffusion have been measured in P3HT, PQT-12, and poly(fluorene) transistors.[39−41] In F8T2-based TFTs, the threshold voltage shift reversed under illumination, and it was determined that bias stress is essentially due to trapping of holes in the polymer rather than in the dielectric.[41] The amount of trapping depends only on the charge concentration in the channel and hence on the gate voltage. The trapped charge causes a V_T shift toward negative voltage, and, as a result, the on-current is lower than expected and the transfer characteristics are nonlinear and show pronounced hysteresis. On the basis of trapping kinetics, Street et al. have proposed that the bias stress mechanism in polymers consists of the pairing of mobile holes into self-trapped bipolarons.[42]

To minimize bias stress, the carrier concentration in the channel must be kept as low as possible. This requirement is problematic because a high carrier concentration is needed with materials with low mobility to provide a current of ~2 μA to drive pixels in a sizeable display at video rate. These two apparently

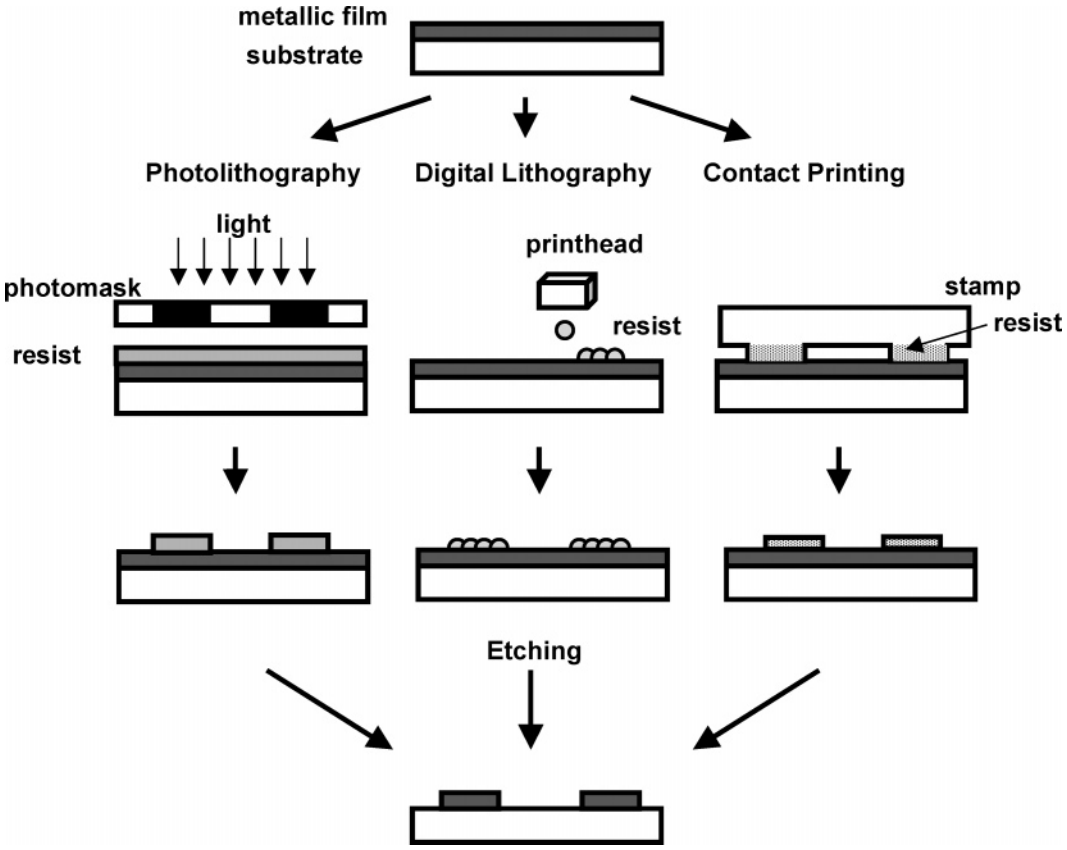


Figure 4. Schematic of three patterning schemes for conductors. The fabrication steps for the photomask used in photolithograpy and the stamp used in contact printing have been left out. The need to fabricate a master increases the number of processing steps needed for these techniques relative to digital lithography.

conflicting requirements can be met simultaneously only by increasing W/L. For example, in F8T2, a $(W/L)_{min} \approx 80$ is needed to run a 600 line display at video rate and simultaneously keep the TFTs below the onset of bias stress.[41] Therefore, the onset of bias stress instabilities may place additional constraints in the choice of the appropriate semiconductor or device geometry.

III. Fabrication Processes for AM-OTFT Backplanes

Overview. The fabrication of AM-TFT backplanes requires deposition and patterning of thin (~100 nm) layers of conductors, dielectrics, and semiconductors. In a typical design, the dielectric layer is essentially unpatterned, and the conductors and semiconductors are patterned on a fine scale (1−10 μm).[5] The micrometer-scale features must also be registered with respect to each other over the vertical layers of the backplane structure to tolerances of ~5 μm. Due to the sensitivity of organic semiconductors to organic solvents,[44] ionic impurities,[39] and thermal cycling,[13,16] research that examines the performance of OTFTs fabricated with new processes is important for the development of organic AM-OTFT backplanes.

All AM-TFT backplanes in production are fabricated by depositing layers using vacuum or plasma enhanced chemical vapor (PE-CVD) methods and by patterning these layers using photolithographic methods.[9] Photolithographic patterning is typically performed by (i) coating a resist, an organic polymer, on a layer, (ii) exposing the resist to light that is transmitted through a photomask, (iii) developing the resist to reveal the pattern, and (iv) etching the exposed material using wet or dry methods (Figure 4).[4] These methods can fabricate 3 μm features that are registered to within 0.6 μm on large substrates (~1.8 m × 2.2 m) through the use of precise optomechanical projection systems.[45] The main drawback of these technologies is cost. Reactors used to deposit high electrical quality films using PE-CVD are expensive and are difficult to scale to very large areas (>1 m^2).[46] In production, reductions in processing steps used for deposition and patterning can lead to reductions in cost.

Alternative methods of patterning from the printing industry are being examined to replace photolithographic patterning. Printing methods, such as flexographic marking and jet printing, are used routinely to make large-area, low-cost high-resolution documents and graphics. Important questions for these technologies are whether they can achieve the multilevel registration (better than 10 μm) required for backplanes and whether they can be performed in high yield with very low numbers of defects.

We outline the progress in the deposition of and the patterning methods for materials used in AM-OTFT displays in the following section. These patterning methods can be classified into two categories, subtractive and additive methods. Subtractive methods deposit a blanket layer of material and remove the majority of it to define a feature. For example, photolithography is a subtractive patterning method. Additive methods deposit only enough material to create a desired feature.

It would be advantageous to have a fabrication process where all of the steps are additive because of the reduced waste and a potential reduction in the total number of fabrication steps. This section is not a comprehensive review, but represents an overview of printing processes that have been used to successfully fabricate structures used in AM-OTFT backplanes.[47]

A. Conductors: Gate and Data Levels. AM-TFT backplanes have two separate layers with conductive electrodes, the gate level and the data level, which contain the source and drain contacts of the TFTs.[5] While the conductors on these levels have similar requirements for absolute conductivity, they have different materials requirements. Most organic semiconductors are hole conductors and thus require the use of a source electrode with a high work function. The choice of material for the gate electrodes is constrained by compatibility with the gate dielectric material. In addition, the gate electrodes must be thin enough to ensure good coverage by the dielectric material over their edges.

Contact Printing. Contact printing comprises a set of patterning methods where a pattern of ink is defined on a flexible stamp and then transferred to a substrate by mechanical contact (Figure 4).[48] The stamp may be directly patterned with features, inked, and then placed into contact with a substrate, such as in flexographic printing, or the ink may be transferred from a rigid, patterned master to a flexible transfer surface that is placed in contact with the substrate, such as in offset printing. Because contact printing is purely mechanical, no optical exposure system is required to define a pattern, reducing the complexity of the patterning tool.

Offset Printing. One of the first printing methods examined to pattern conductors in large AM-TFT backplanes was offset printing.[49] A UV-curable ink was placed in patterned wells in a rigid glass plate and then transferred to a silicone-based roller that was placed into contact with a metallic film. The transferred ink was then cured by UV exposure and used as a wet etch resist. Features of 35 μm with separations of 10 μm were created in metals and silicon using this technique. While this method was used successfully to fabricate poly-Si TFTs, its further use requires exploration of inks that are adequate etch resists and have low ionic impurities, which can contaminate dielectric and organic semiconducting layers. The physical limits of microscale offset processes have been examined and depend critically on the capillary, viscous, and adhesive forces on the ink.[50]

Soft Lithography. Soft lithography comprises a variety of patterning methods whose common feature is the use of an elastomeric stamp, typically made of a poly(dimethylsiloxane) (PDMS). These methods have been extensively reviewed,[48,51] and we focus here on the variations that have been demonstrated for the fabrication of OTFTs.

Microcontact Printing (μCP). One of the most widely researched techniques for patterning metallic conductors is the printing of a patterned SAM of an organothiolate that is used as a wet etch barrier on a metal (Ag, Au, Pd, Cu).[51] Micrometer-scale features with edge resolutions of ~200 nm with gold and ~75 nm with palladium can be readily patterned (Figure 5).[52] The drawback of the use of SAMs as etch resists is the limited number of metals that can be patterned. The gate electrodes of an AM-TFT backplane are typically fabricated from Al or MoCr due to their low cost, high conductivity, and compatibility with PE-CVD deposited dielectric layers.[5] Coinage metals can diffuse into oxides to form charge traps, which in turn affect the electrical performance of TFTs. The extension of μCP to metals outside of the coinage series would be advantageous for the fabrication of gate electrodes. Fortunately, gold is commonly used for the source and drain electrodes in OTFTs.

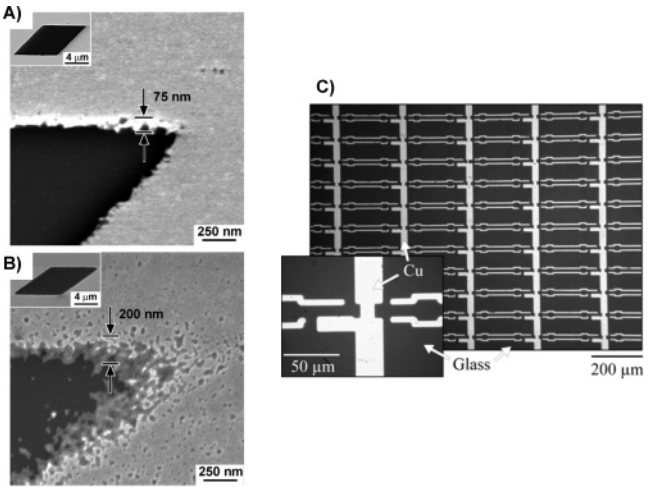


Figure 5. Scanning electron micrographs of metallic films patterned by microcontact printing. (A) Patterned layer of palladium.[52] (B) Patterned layer of gold.[52] (C) A patterned layer of electroplated copper suitable for the gate electrode layer of a AM-TFT backplane.[54] (A, B) Reprinted with permission from ref 52. Copyright 2002 American Chemical Society. (C) Reprinted with permission from ref 54. Copyright 2003 American Chemical Society.

Microcontact printing has been used to fabricate both the gate and the data levels of prototypes of AM-TFT backplanes. The IBM group has developed a μCP-based process for gate electrodes based on etching of an electroplated copper layer.[53] They used electroplated Cu layer as an etch mask for an underlying electrolessly plated NiB layer (Figure 5).[54] After definition of the NiB electrodes, they removed the Cu layer by wet etching leaving only the NiB layer. This process has been performed on 15-in. glass substrates. Rogers and coworkers have fabricated the source and drain level electrodes of an AM-OTFT backplane using gold electrodes that were patterned by μCP.[55] They patterned ~10 μm features with registration of ~50 μm to electrodes defined by photolithography on a 5-in. × 5-in. substrate. In other work, a gold film supported by a PDMS film was patterned by μCP and then laminated onto an organic film to form the source and drain contacts of a TFT.[56] This method creates a staggered OTFT, a structure that typically has lower contact resistance than a coplanar structure.

The main challenges for soft lithographic techniques are the fidelity of patterned features and registration over multiple patterned levels. The mechanical properties of the elastomeric stamp must be tuned to promote conformal contact with the substrate and to prevent distortions in the printed features due to deformation upon contact.[48] The mechanical properties of PDMS stamps can be improved by using highly cross-linked

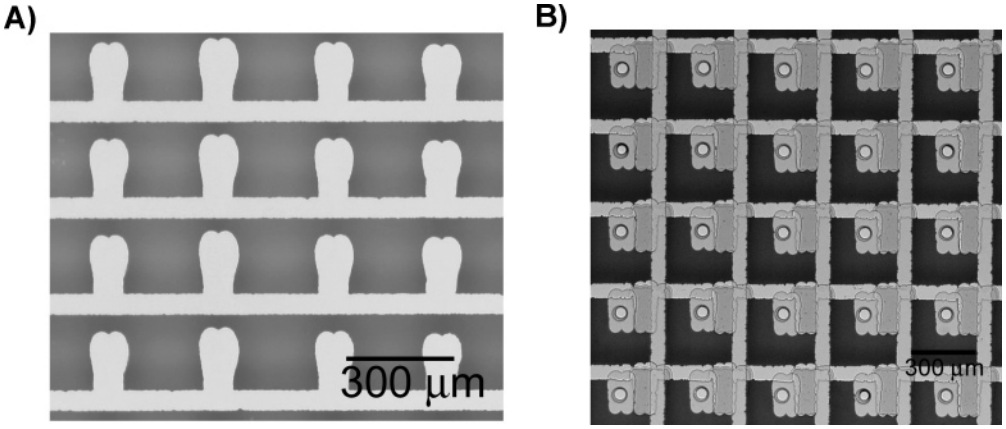


Figure 6. Optical micrographs of metallic layers patterned using digital lithography.[60,61] (A) A patterned chromium film used for the gate electrode layer of an AM-TFT array. (B) A finished a-Si:H-based AM-TFT array showing the multilevel registration of digital lithography.

varieties of PDMS[57] and by using two-layer stamps where the PDMS was supported by a stiff polymeric, metallic, or glass support.[48] A method referred to as "wave printing" that uses a traveling air pressure wave to press a stamp into contact with a substrate has been shown to reduce distortions.[58]

Direct Marking. Direct marking of materials is a more efficient patterning method than photolithography and contact printing because no material is wasted. Direct marking methods, such as inkjet printing, are particularly flexible because they can deposit a digitally defined pattern, that is, one stored on a computer. The main challenge for inkjet printing is control of the printed liquid drop.[59] The volume of a drop ejected from a high-resolution printer is ~10−100 pL. The final size of the feature is controlled by spreading of the deposited drop on the substrate. Registration to previously patterned layers is controlled by physical alignment and by spreading of the drop on the substrate.[59]

Digital Lithography. We refer to subtractive techniques in which a resist is directly deposited from a printer as digital lithography. One of the first examples was the use of a xerographic printer to fabricate amorphous silicon TFTs.[1] A patterned toner layer was deposited onto a thin glass substrate and used to lift-off a metal evaporated onto it. The subsequent layers of the TFTs were patterned by printing toner onto a flexible substrate and then transferring it to the substrate to be patterned using heat and mechanical pressure. The transfer printing step was necessary to achieve alignment to the initial layer. This strategy resulted in line widths of ~300 μm and registration of ~100 μm.

Wong and co-workers at PARC have recently demonstrated a digital lithographic process that uses wax-based resists for patterning conductors.[60,61] Wax undergoes a solid-to-liquid phase change at relatively low temperatures; the phase change can be used to control the feature sizes of the printed wax by precise control of the temperatures of the printhead and substrate. Feature sizes of 20 μm have been demonstrated with 40 μm used routinely (Figure 6). In this work, the existing patterned layer on a substrate was digitally imaged prior to the next printing step. Digital imaging of the substrate prior to deposition allows software adjustment of the mask layer yielding very good multilayer registration (~5 μm). This technique has been used to pattern conductors for both amorphous silicon[61] and AM-OTFT backplanes.[62]

Directly Printable Conductors. A number of workers have examined printable metallic conductors. The formation of a continuous film from thermal processing of a metallic precursor is challenging; organic materials used to stabilize the metallic species can cause void formation or chemical impurities in the metallic film and reduce its conductivity. Wagner and co-workers have printed a solution of copper hexanoate in 2-propanol and thermally transformed the printed material into metallic copper at 200 °C. [63] The printed electrodes were 6 times more resistive than those made from bulk copper. The use of metallic nanoparticles, that is, particles with sizes of ~1−5 nm, can reduce the temperature needed to form the continuous film. Subramanian and co-workers have printed alkanethiolate-protected gold nanoparticles and sintered them at ~150 °C to fabricate lines with widths of ~100 μm and thicknesses of ~1 μm, and conductivities within ~70% of bulk films.[64]

The most widely used, stable, organic conductors have low conductivities relative to metals (~10^4 times lower), but make good electrical contact to organic semiconductors. Direct printing of a blend of PEDOT:PSS has been used to fabricate conducting contacts (~10 S/cm) to all-polymeric TFTs.[65] To achieve the high-resolution features needed for source-drain contacts, the wettability of the substrate was prepatterned by lithography to control the size of the printed feature. Gaps between PEDOT:PSS electrodes as small as ~100 nm have been achieved using this hybrid method.[66] Dupont has demonstrated large-area printing of a composite film of polyaniline and single-wall carbon nanotubes; the composite has a maximum conductivity of 2 S/cm.[67] They have patterned this material over large areas (50 cm × 80 cm) by laser transfer of 5 μm × 2.7 μm pixels from a dry solid film to a substrate.[67] While organic materials may be used as contacts, it is unlikely that they can be used for addressing lines in large AM-OTFT backplanes unless materials are developed that have conductivities approaching those of bulk metals.

B. Deposition of Gate Dielectric Layers. The main issue in the fabrication of the gate dielectric layer is the choice of material. Inorganic insulators have good

electrical stability and low leakage currents (<10 pA/cm^2), are impervious to organic solvents, and are stable in a wide range of environments. One of the main disadvantages of inorganic dielectrics is the deposition temperature; continuous films without large amounts of trapped charge or shallow traps are typically obtained at temperatures above 150 °C. Deposition of good electrical quality films at low temperatures is difficult, but possible.[68]

In an effort to move away from the complexities of inorganic materials, research in organic polymeric dielectrics is increasing.[69,70] The design of an organic dielectric is difficult because compatibility with the organic semiconductor must be considered. Because polymeric semiconductors are typically dissolved in aromatic solvents, Sirringhaus and co-workers chose a top-gate geometry so that the dielectric polymer, poly(vinylphenol) dissolved in 2-propanol, could be spun on top without damaging the semiconducting layer.[65] Another solution is to fabricate a cross-linkable polymeric film that can withstand subsequent processing steps with organic solvents.[69,71] A cross-linked copolymer of poly(vinylphenol) and poly(melamine-*co*-formaldehyde) has been used as a gate dielectric for TFTs fabricated with vapor-deposited pentacene and oligothiophenes.[71] The TFTs made with pentacene were reported to have $\mu = \sim 0.2$ cm^2/(V s) and gate leakage currents of $\sim$100 nA/cm^{-2}. Vapor deposition of otherwise intractable organic materials, such as parylene, has also been demonstrated.[10,72] While there have been a number of reports of OTFTs with good performance using organic dielectrics,[71] there are few reports of their electrical and environmental stability.[73,74]

C. Deposition and Patterning of Organic Semiconductors. The semiconducting layer of a TFT is the most challenging layer to deposit and to pattern. The performance of this layer is extremely sensitive to electrically active impurities and to the interfacial structure between the semiconductor and the dielectric. The patterning methods for organic semiconductors are constrained by the choice of deposition from solution or vapor.

Patterning of Vapor-Deposited Semiconductors. Films of molecular semiconductors, such as pentacene, are difficult to pattern using solvent-based methods due to their mechanical and chemical properties. Exposure of films of pentacene to common organic solvents such as acetone and 2-propanol causes changes in the morphology of the film and can reduce the mobility of the material by almost a factor of 10.[44] The use of a vapor-deposited encapsulant, such as parylene, has been demonstrated to partially protect pentacene from solvents during wet processing; the degradation of the mobility of the TFTs after organic solvent washes was reported to be a factor of $\sim$2.[75] A patterning process that uses oxygen plasma-based etching of pentacene film with regions protected by a film of a poly(vinyl alcohol) has been reported.[76,77] In this work, some degradation of the electrical properties was observed upon subsequent processing despite the protective layer.

Vapor-deposited organic films are commonly patterned using a shadow mask or aperture mask. The scale of features formed under the aperture is affected by the distance between the mask and substrate, the collimation of the source vapor, and the aperture size.[78] The difficulties encountered with aperture masks include the fabrication of large area masks, placement of the mask within close proximity of the substrate, and registration to previously patterned features. Rogers and co-workers used shadow masks to define the pentacene layer in a AM-TFT backplane for electrophoretic media.[55] In these arrays, the gate electrodes were large ($\sim$500 μm), so alignment between the semiconductor and gate region was not critical. Baude and co-workers at 3M have used flexible shadow masks fabricated from Kapton where the apertures were created by excimer laser ablation.[79] The masks were used to fabricate features sizes of $\sim$10 μm with registration of $\sim$30 μm. They have used this method to pattern layers of pentacene as well as conductors and dielectrics deposited by vapor deposition. In both of these reports, the pentacene layer was encapsulated with a vapor-deposited inorganic layer after its deposition.

Scheme 1

An alternate method to thermal deposition from vacuum is to use an inert carrier gas to transport the organic material from a heated source to a substrate; this process is referred to as organic vapor phase deposition (OVPD).[78] Patterning of films deposited by OVPD can be achieved using an aperture mask similar to that used in simple thermal deposition.

Patterning of Solution-Processed Semiconductors. The ability to deposit semiconductors from solution is advantageous because of the number of patterning methods that are available. The use of a solvent, however, complicates the fabrication of high performance TFTs. Molecular ordering is a critical factor affecting field effect mobility, and it can be difficult to control both the uniformity and the crystallinity of films of small molecules and polymers deposited from solution. In addition, if a solution-processed dielectric is to be used, it must not be soluble in the solvent used to deposit the semiconducting material.

Photolithographic Patterning. Due to the prevalence of photolithography in semiconductor manufacturing, many groups have worked toward methods to pattern organic semiconductors using resists and etching or by making an inherently photosensistive material. The latter is challenging due to the possibility of unreacted or residual impurities creating electronic traps or doping the semiconducting layer.

Philips has done extensive work to demonstrate the compatibility of organic semiconductors with conventional photolithographic methods.[8,74] They have used solution-processable forms of pentacene[80] and PTV.[8] These materials are normally intractable, but precursors with thermally removable, solubilizing groups have been developed (Scheme 1). These materials were not engineered to be intrinsically photopatternable and were patterned using conventional photolithographic methods after the thermal conversion. After patterning, TFTs made from a precursor of pentacene had $\mu = 0.02 \pm 0.004$ cm^2/(V s) and off-currents of $\sim$1 pA.[74]

The development of a photosensitive semiconductor would reduce the complexity of photolithographic pat-

terning. The challenge is the development of a material that can either be rendered nonconducting or be removed by a development step after exposure to light. These requirements present difficulties in designing a material for the semiconducting layer of a TFT because the concentration of electronic traps must be very small. Recently, a photosensitive pentacene precursor has been developed by Afzali and co-workers at IBM;[81] feature sizes of 10 μm were fabricated by direct photolithography, and the finished TFTs had $\mu = 0.015$ cm^2/(V s).

Contact Printing. A number of workers have explored the use of soft lithographic techniques to pattern polymeric layers.[82] A typical strategy is to spin coat a solution containing the polymeric material onto a PDMS stamp, to allow the liquid to dry, and then to transfer the film to the substrate. Park and co-workers have fabricated P3HT-based TFTs using such a method and obtained devices with $\mu = 0.007$ cm^2/(V s) and on-to-off ratios of 10^2 with a polyimide-coated silicon oxide gate dielectric.[83] A difficulty with this process is the incompatibility of many organic solvents with PDMS that can cause distortions in the features of the stamp.[84]

Integrated Microfluidic Channels. Chabinyc and co-workers at PARC have fabricated 64 × 64 arrays of TFTs using polymeric microfluidic channels that are aligned to the data electrodes of the array.[85] A solution of the polymeric semiconductor was drawn through the microfluidic channels by passive capillary action. This method has been demonstrated to produce OTFTs with $\mu = 0.05$ cm^2/(V s) and on-to-off ratios of $>10^7$ with PQT-12.

Jet Printing. Jet printing of semiconducting materials has the same advantages as digital lithography for registration; digital imaging of the substrate prior to deposition allows software adjustment of the printed pattern, yielding very good multilayer registration. The largest effort in jet printing conjugated polymers has been in the area of organic light emitting diodes (OLEDs) for emissive displays.[86] The performance requirements of the semiconducting layer in OLEDs are quite different from those in TFTs. The materials for OLEDs are typically amorphous, and the main concern is optimization of drying conditions to obtain uniform thickness of the dried films. In contrast to OLEDs, molecular ordering is critical to the performance of OTFTs, and deposition conditions may have a dramatic effect on performance.

A number of groups have reported work on jet printing of organic semiconducting materials for TFTs. Plastic Logic has reported jet-printed F8T2 TFTs with feature sizes of ~100 μm using a piezoelectric printhead onto glass substrates.[66] The reported characteristics of these TFTs were $\mu = 0.008$ cm^2/(V s) and on-to-off ratios of 10^5. Paul and co-workers at PARC have printed PQT-12 and F8T2 using a printhead that uses acoustic waves to eject drops. They achieved dried spot sizes of 35 μm on common gate structures and were able to obtain registration of 10 μm.[87] The performance of these TFTs was identical to that obtained from spin coating these materials on the comparable substrates (for PQT-12, $\mu = 0.08$ cm^2/(V s) and on-to-off ratios of 10^7). Subramanian and co-workers have used a piezoelectric printhead to deposit a solution-processable form of pentacence.[88]

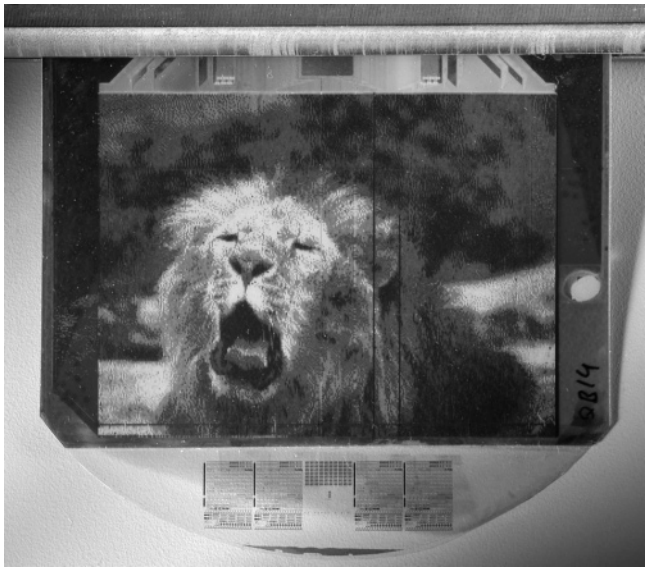


Figure 7. Finished electrophoretic quarter-VGA display with a flexible AM-OTFT backplane patterned by photolithographic processing. Photograph courtesy of Polymer Vision (www.polymervision.com).

They did not report feature sizes, but obtained TFTs with $\mu = 0.02$ cm^2/(V s) and on-to-off currents of 10^5.

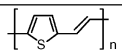
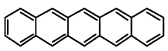
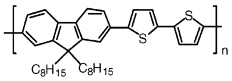
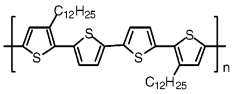
While jet printing has been demonstrated to fabricate high performance OTFTs, development of these methods is needed. Most organic semiconductors are soluble in aromatic solvents that are incompatible with many printheads due to the gaskets and epoxies that are used to fabricate the instrument.[89] Printing in the ambient environment also requires the synthesis of stable organic semiconductors. Control of feature sizes and multilevel registration is challenging; nearly all solution-processable organic semiconductors perform best on dielectrics with hydrophobic surfaces, and it is difficult to control drop placement on these surfaces due to their poor wettability and the momentum of the jetted drop.[59]

IV. Summary and Outlook

A number of groups have demonstrated completed AM-OTFT backplanes using the techniques and knowledge of device characteristics reviewed here (Table 1). The majority of workers have used photolithography to pattern layers in these devices and used pentacene as the semiconductor. For example, Philips has demonstrated plastic AM-OTFT backplanes patterned by photolithography that can drive electrophoretic media in a quarter-VGA display (Figure 7).[74] There are two examples where no photolithographic patterning was used. PARC reported an all print-patterned 128 × 128 pixel AM-OTFT backplane where the metallic conductors were patterned using digital lithography and the semiconducting was jet-printed (Figure 8).[62] Dupont and Bell Labs reported a 50 cm × 80 cm backplane fabricated using dry-transfer printing of conductors and an evaporated semiconducting layer. Despite the differences in the methods chosen in all of these reports, they demonstrate how multiple processes and materials can be integrated to fabricate AM-OTFT backplanes.

There are many areas that must be researched to improve AM-OTFT backplanes. Our understanding of

Table 1. List of Published Completed AM-OTFT Backplanes

Number of pixels	Pixel resolution (dpi)	Semiconductor	Mobility $cm^2/(V\ s)$	W/L	Patterning methods used in overall process	Ref.
64x64	50	 PTV	0.0015	80	Photolithography	7, 8
16x16	~3	 Pentacene (vapor)	0.1	10	Photolithography μCP Shadow Mask	55
16x16	100	Pentacene (vapor)	1.2	20	Photolithography	76
100 x 50	~3	Pentacene (vapor)	0.3	10	Dry Printing Shadow Mask	67
60x80	50	 F8T2	0.008	20	Photolithography Jet-printing	66
320x240	68	Pentacene (from precursor)	0.02	80	Photolithography	74
128x128	75	 PQT-12	0.06	1.5	Jet printing	62

the electrical stability of OTFTs is in its infancy; it is unknown whether improvements in chemical structures or in synthetic methods and purification techniques for organic semiconductors[90] will solve problems such as bias stress. The development of organic semiconductors with resistance to solvent washes and environmental stability will increase the number of options for processes for fabrication. Even with improved environmental stability, compatible encapsulants will also be needed for AM-OTFTs backplanes to protect the organic semiconducting material over long time scales.

One of the most important needs for the future is further development of patterning and deposition processes for flexible substrates that will aid in roll-to-roll manufacturing of backplanes.[46] Structural polymers with high thermal stability, low coefficients of thermal expansion, and low moisture permeability must be developed for these processes. New organic dielectrics and processes to deposit inorganic dielectrics at low temperatures on these substrates must be developed. The use of flexible substrates for AM-OTFT backplanes will also require research on the electrical behavior of organic semiconductors under mechanical stress.

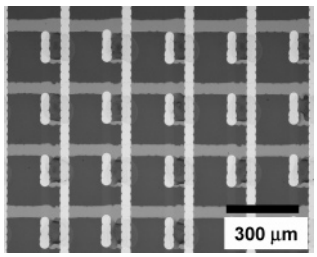


Figure 8. Optical micrograph of a section of a 128 × 128 array of OTFTs on glass. The conductors were patterned using digital lithography,[60,61] and the PQT-12 semiconducting layer was jet-printed.[62]

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